REMARKS/ARGUMENT

The objections to the drawings are believed obviated by the submission herewith of formal drawings in which the Examiner's suggested changes have been adopted.

Similarly, the objections to the specification are believed obviated by the above amendments to the specifications in which the Examiner's suggested changes have been adopted.

The objections to the claims are believed obviated by the amendments to claims 2, 5 and 6, which follow the Examiner's suggestions.

The rejection of claims 1, 2, and 4 - 7 under 35 U.S.C. 103(a)as being obvious variously over Mimura (US 6,249,643) in view of Ochi (US 4,542,409), over Mimura in view of Ochi, further in view of Ackland (US 5,576,763), and over Ackland in view of Ochi, are respectfully traversed. Mimura regards the signal processing needed at the instance when a sensor arrangement is used, and the signal processing has the pattern shown in Figure 2(a). Because of the sensor arrangement, the subsequent signal processing is made more challenging and the patent addresses this signal processing technique. In this sensor arrangement, the effective scan - for both fields of the interlaced frame - is a "zig-zag" or serrated pattern as shown by the solid arrows for one field and the dashed arrows for the other field. In fact, Mimura does not suggest, teach or infer any details of the sensor, and in fact, is probably limited to use only in a CCD implementation, and not CMOS as in the subject application. The signal read-out details are therefore completely lacking.

On the contrary, in the subject patent application, the normal rectangular pixel arrangement is described (that is suitable for implementation in a CMOS sensor) which has the scanning following a zig-zag pattern only during one of the fields (as shown in Claim 1 ("said first and second light detecting elements in two adjacent rows disposed in a serrated manner are activated by second read lines to generate even field signals") and Fig. 4). That is, the even field is the one that is used (as an example) with the zig-zag arrangement to emulate a sensor row positioned half way between the rows for the odd field, whereas the odd field is scanned in the normal linear fashion. Mimura is therefore not applicable to the subject application, as the alternating straight and zig-zag scans and the resulting physical and electrical advantages as described in the subject application are not taught by Mimura.

Ochi uses a linear scan, without the zig-zag arrangement on either of the odd and even fields of the image frame. The arrangement is set so that two pixels are connected to two column lines during one field and another set of two pixels are connected to two column lines during the opposite field. The resulting offset is one pixel vertical pitch between the even and odd fields. In Ochi, the use of the parallel transistors (as compared to the prior art described in Ochi) is to reduce pixel complexity only, by merely eliminating an interconnecting line.

In comparison, the arrangement of the subject patent application is described as allowing the offset to be one-half the pixel vertical pitch due to the zig-zag scanning during one of the fields. In addition, only one column line is used. For these reasons, the subject patent application is significantly different from, and is not obvious in light of Mimura and Ochi.

As explained in the office action, the examiner rejected Claims 1, 4, and 7 based on the relevant portions of Mimura and Ochi that he highlighted, such as Figs. 1, 2(b), 4, and 5(a), and column 2, line 64 to column 3, line 3 of Mimura and Fig. 5 and column 6, lines 10-25 of Ochi. The examiner held that persons skilled in the art can combine the interlaced readout line pattern of Ochi with the image sensor, activated in a serrated manner, of Mimura.

As stated by the examiner, Figs. 5 (a) and 5(b) of Mimura only disclose that signals separated for different fields are double oversampled "only" in a zigzag manner. Mimura teaches away from the technique of selectively activating the first and second light detecting elements by means of the first read lines and second read lines, respectively. According to the subject invention, odd field signals are generated by activating "all" of the first and second light detecting elements "in each row" and then even field signals are generated by activating the first and second light detecting elements in two adjacent rows disposed in a serrated manner (i.e., "the even field is the one that is used with the zig-zag arrangement to emulate a sensor row positioned half way between the rows for the odd field, whereas the odd field is scanned in the normal linear fashion" as stated above).

Given the above, Mimura and Ochi taken alone or in combination do not suggest, teach or motivate Claim 1 and Claim 7 (which is a method claim corresponding to apparatus Claim 1) of the subject application. Also, since Claim 1 is nonobvious over Mimura and Ochi, Claim 4, depending from Claim 1, is nonobvious over Mimura and Ochi as well.

Regarding Claims 2, 5, and 6, Ackland is referred to as teaching the reset and source follower transistor. However, Ackland teaches the physical construction of a specific type of four-transistor pixel using one polysilicon layer. In the subject patent application, it is shown how this type of pixel is incorporated in our concept. This incorporation is not evident from Ackland. However, other pixel arrangements may be also used easily, including the more common three-transistor pixel, and indeed even an arrangement that would share some of the transistors with adjacent rows to reduce the complexity (as referred to in the subject application, lines 17 through 21 of page 5). Given the above, since Claim 1 is nonobvious over Mimura, Ochi, and Ackland, Claim 2, depending from Claim 1, is nonobvious over Mimura, Ochi, and Ackland as well. In addition, Claims 5 and 6 are not suggested, taught, or motivated by the disclosures of Ochi and Ackland.

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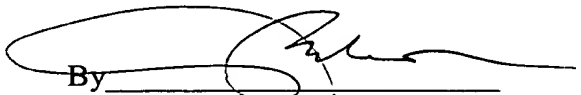
Respectfully submitted,



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